MAINTENANCE MANUAL
LOGIC BOARD
TMX-8415, TMX-8615 & TMX-8630

TABLE OF CONTENTS

DESCRIPTION

The logic board for the TMX-84 and TMX-86 series trunked mobile radios controls the operation of the radio. The logic board provides all of the necessary analog/digital processing, tones, codes and control functions. The logic circuitry controls channel acquisition, RF frequency selection, tone/code generation and detection, and operator interface functions. Interface functions include control panel displays and switch panel, audible alert tones, and test handset and programming functions.

The logic board contains the microprocessor, digital signal processor, external memory EPROM for the microprocessor, the programmable personality EEPROM, and two octal latches for the I/O microcomputer interface.

The logic board is mounted in the top section of the chassis above the transmitter/receiver/synthesizer (TRS) board. All power and control function interconnections are provided by cables CA11, CA12 and CA13.

Simplified diagrams and pin-out information on the Integrated Circuits are contained in the Service Sheet listed in the Table of Contents.

CIRCUIT ANALYSIS

The logic board contains the digital processing and initializing circuitry for the trunked mobile radio.

Digital processing circuitry consists of microprocessor A1, octal latches A2 and A11, EPROM A3, EEPROM 4, digital processor A5 and CODEC A6.

A3 is an 8K x 8 bit EPROM. It is used by the microcomputer to control all radio and system functions. Crystal Y1 and inverter A14 provide the time base to sequence the microcomputer through its internal software program, allowing it to execute the program stored in the program memory.

EEPROM A4 contains all data unique to the radio and is referred to as the Personality PROM. Information stored in the Personality PROM includes all area and group information (including RF channels and signalling tones) as well as all radio options (e.g. carrier control timer, hookswitch options, alert tone control, etc.)

A5 is a digital signal processor used to generate and detect signalling tones, provide filtering and control the exchange of serial data to and from CODEC A6. The digital processor utilizes 8 parallel data lines to interface with the microcomputer.

A simplified diagram of the digital processing circuitry is shown in Figure 1.

Power for the logic board is provided by a continuous 13.8 volts (A+), a switched 13.8 volts (SW A+), and a regulated +5 volts (Vcc) from the TRS board. A regulated +5 volts DC and -5 volts DC is derived from the switched A+.

OCTAL LATCHES A2 & A11

Octal latches A2 and A11 are used to exchange data passing between microprocessor A1, and the memory and control circuits respectively.

GENERAL ELECTRIC

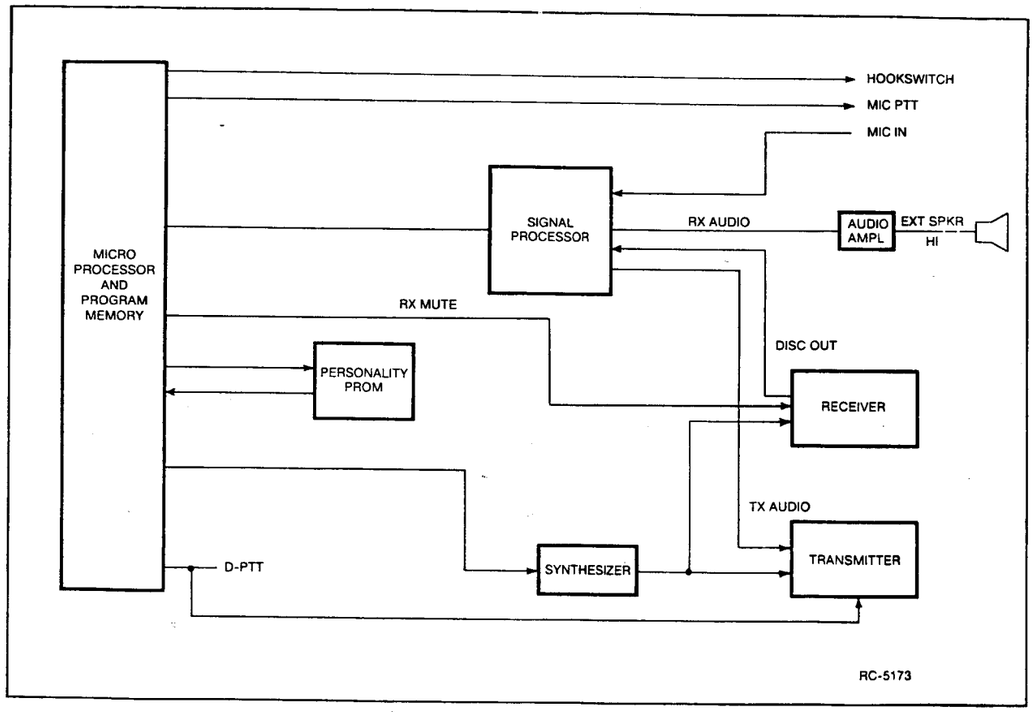

Figure 1 - Simplified Digital Processing Diagram

Octal latch A11 provides the interface between the microprocessor and the control panel switches. A11 is connected so that the latch function is disabled (the "G" input A11-11 connected to 5 volts) and the octal latch operates as a buffer for the microprocessor output.

Octal latch A2 has the "G" input connected to the ALE (address latch enable) output of the microprocessor to provide a latched address interface between the EPROM, and personality EEPROM.

RESET/MEMORY BACKUP

The microprocessor reset and memory backup circuit consists of 5-volt regulator A16, zener diode CR2, switching transistors Q1 and Q2, and pass transistor Q3.

Microprocessor A1 is reset by switched A+ (13.6 volts) on/off and programmer reset. The microprocessor resets when +5 volts is applied to RST input A1-9 from regulator A16 through pass transistor Q3.

In a power-down state (A+ SW off), zener diode does not conduct, keeping Q1 turned off. When Q1 is off Q2 conducts, turning on Q3. Turning on Q3 applies +5 volts from the collector of Q3 to reset pin 9 of U1. The 5-volt supply provides the memory backup for microprocessor A1, and keeps A1 in the reset state.

When the radio is turned on (A+ SW on), zener diode CR2 conducts, turning on Q1. Turning on Q1 turns Q2 and Q3 off. The +5 volts to A1-9 decays to about 0 volts as determined by the time constant of C3 and R6. When the voltage at A1-9 drops to approximately 0 volts, the microprocessor starts executing its program memory approximately 12 milliseconds after Q1 turns on and Q2 and Q3 turn off.

MICROPROCESSOR A1

Microprocessor A1 directly interfaces with and controls the operation of all the digital processing circuitry. It also interfaces with the radio and control panel display functions through octal latch A11 and external buffer stages.

The microprocessor controls the operation of the radio by performing the following major functions:

- System Timing
- Frequency Selection
- Mode Selection
- Group Selection
- Transmit/Receive Control
- Test Handset Control and Display
- Audio Routing and Mute Control
- Maintenance Functions

Microprocessor A1 is sequenced through its program by an internal oscillator whose frequency is set by crystal Y1. The oscillator frequency is 8.192 MHz.

The microprocessor accesses its program memory from EPROM A3. Reading of the stored program at A3 occurs when the PSEN line of A1 is low. The upper eight address lines of A1 (A8-A15) are stationary during this access time. The lower eight address lines of A1 (AD0-AD7) are captured by octal latch A2 and held stationary. ALE (A1-30) is used to latch the lower eight address lines. The output of A3 is then read into the data bus (AD0-AD7) of A1.

The microprocessor interfaces with the microphone through MIC PTT and LOGIC HKSW. It also interfaces with the TQ2310 programmer through HKSW, MIC PTT, SER DAT and SP RESET on P1, and with the digital signal processor A5, and Personality EEPROM A4.

The microprocessor control signals include the following:

$\overline{EA}$ (Enable) - When low allows microcomputer to retrieve all instructions from external memory.

$\overline{RST}$ (Reset) - Resets microcomputer to beginning of software program when switched A+ is turned off, immediately following power interruptions or with low battery voltage. Also resets when a RST signal from the programmer is received.

SYN DATA - Data transferred to synthesizer representing RF frequencies.

SYN CLOCK - Timing output to synthesizer.

SYN LOCK - A status input signal from the synthesizer to indicate frequency lock status of VCO.

RX MUTE (Receiver Mute) - Turns receiver audio off while operating in the trunked mode during channel acquisition (idle and wait mode) and when transmitting.

D-PTT (Delayed PTT) - Energizes the antenna relay, and turns off the receiver front end and 1st RF amplifier. D-PTT also switches the bilateral audio gates on the logic board in the transmit and receive mode.

$\overline{MIC\ PTT}$ - The microprocessor monitors the status of the switched PTT lead from the microphone. It also receives clock data on this line while the radio is being programmed.

$\overline{RD}$, $\overline{WR}$ (Read, Write) - Allows the microprocessor to read/write data to/from EEPROM A4 and read/write from/to digital processor A5.

PSEN (Program Send Enable) - Allows the processor to read instructions from program memory A3.

ALE (Address Latch Enable) - Allows microcomputer to hold the eight least significant lines (AD0-AD7) stable by using octal latch A2. This is necessary when reading from program memory A3 or reading/writing from/to EEPROM A4.

A8-A15 (Address Lines) - Eight most significant address line. These are used to address and access the program memory, digital processor, and the EEPROM.

DIGITAL PROCESSOR A5

Digital processor A5 is a program-masked IC that operates under the control of microprocessor A1, and performs all processing on the digitized audio serial data stream from the CODEC, A6. The following functions are performed by the digital processor.

- Busy Tone Notching
- Signaling Tone Detection
- Busy Tone Detection
- Alert Tone Generation
- Receive Audio Processing
- Transmit Audio Processing
- Transmit Audio Pre-emphasis
- Transmit Audio Limiter
- Busy Tone Injection
- Tone Generation

The digitized CODEC output is applied to A5-21 (Signal Input), and the processed output is applied to the CODEC on A5-22 (Signal Out). A simplified diagram of the digital processor is shown in Figure 2.

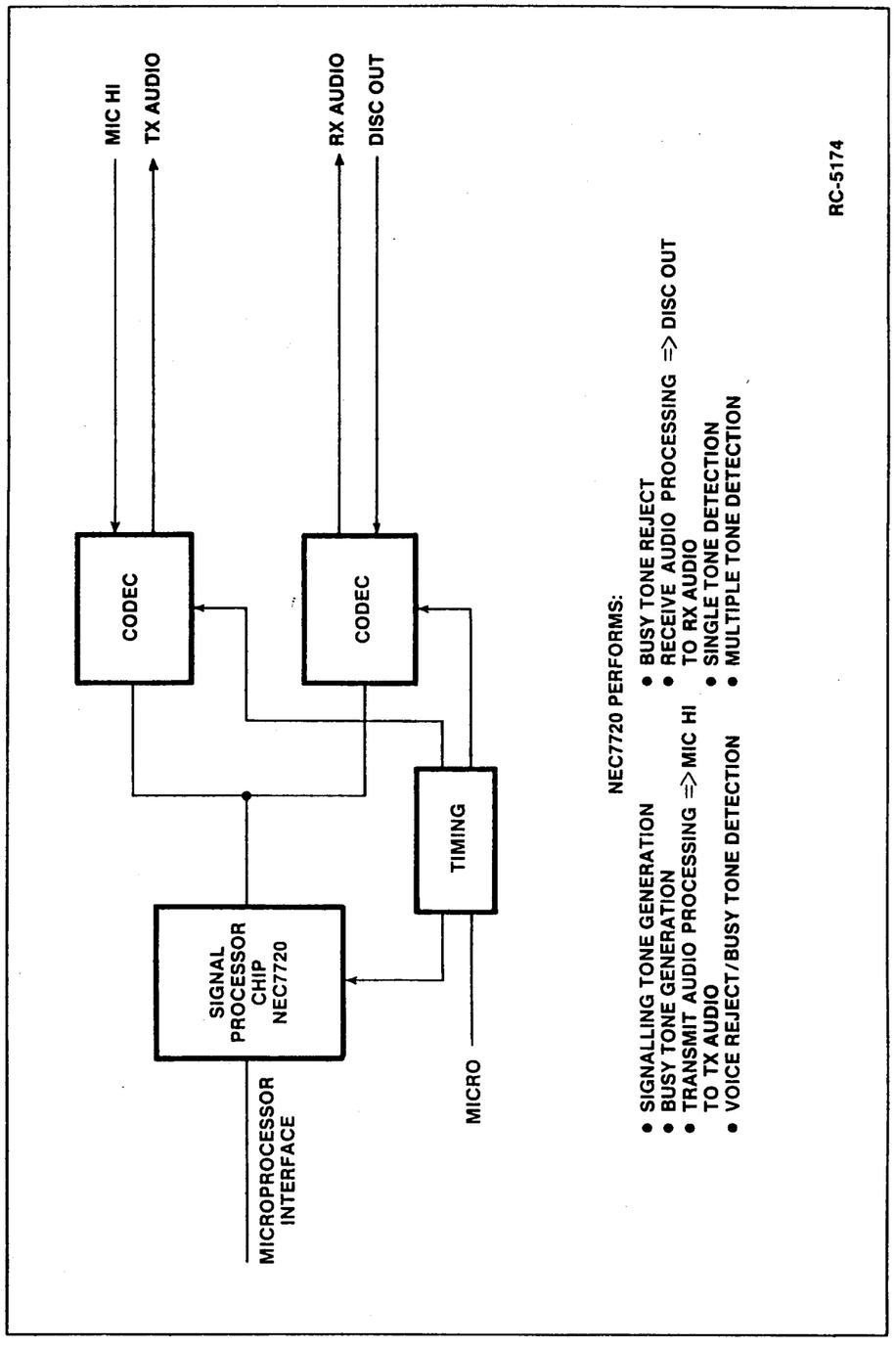

Figure 2 - Simplified Digital Processor Diagram

CODEC A6

CODEC A6 provides the analog-to-digital and digital-to-analog conversions.

The following major functions are provided:

- Bandpass filtering of the analog signals prior to encoding and after decoding
- Encoding and decoding of voice and call progress information
- Encoding and decoding of the signalling and supervision information

Refer to Service Sheet for a Block Diagram of the CODEC A6.

The CODEC can be powered up by pulsing FSx and/or FSr while a TTL high voltage is applied to $\overline{PDN}$, provided that all clocks and supplies are connected. The CODEC has internal resets on power up (or when Vbb or Vcc are re-applied) in order to ensure validity of the digital outputs and thereby maintain integrity of the PCM highway.

On the transmit channel, digital outputs Dx and $\overline{TSx}$ are held in a high impedance state for approximately four frames (500 us) after power up or application of Vbb or Vcc After this delay, Dx and $\overline{TSx}$ will be functional and will occur in the proper timeslot. The analog circuits on the transmit side require approximately 60 milliseconds to reach their equilibrium value due to the autozero circuit settling time.

To enhance system reliability $\overline{TSx}$ and Dx will be placed in a high impedance state approximately 30 us after an interruption of CLK.

Power Down and Standby Modes

To minimize power consumption, two power down modes are provided in which most functions are disabled. Only the power down, clock, and frame sync buffers, which are required to power up the device, are enabled in these modes. As shown in Table 1, the digital outputs on the appropriate channels are placed in a high impedance state until the device returns to the active mode.

The Power Down mode utilizes an external control signal to the $\overline{PDN}$ pin. In this mode, power consumption is reduced to an average of 5 mW. The device is active when the signal is high and inactive when it is low. In the absence of any signal, the $\overline{PDN}$ pin floats to TTL high allowing the device to remain active continuously.

The Standby mode leaves the user an option of powering either channel down separately or powering the entire device down by selectively removing FSx and/or FSr. With both channels in the standby state, power consumption is reduced to an average of 12 mW. If transmit only operation is desired, FSx should be applied to the device while FSr is held low. Similarly, if receive only operation is desired, FSr should be applied while FSx is held low.

Fixed Data Rate Mode

Fixed data rate timing is selected by connecting DCLKr to Vbb it employs master clock CLK, frame synchronization clocks FSx and FSr, and output $\overline{TSx}$.

CLK serves as the master clock to operate the codec and filter sections and as the bit clock to clock the data in and out from the PCM highway. FSx and FSr are 8 kHz inputs which set the sampling frequency. $\overline{TSx}$ is a timeslot strobe/buffer enable output which gates the PCM word onto the PCM highway when an external buffer is used to drive the line.

Data is transmitted on the highway at Dx on the first eight positive transitions of CLK following the rising edge of FSx. Similarly, on the receive side, data is received on the first eight falling edges of CLK. The frequency of CLK must be 2.048 MHz. No other frequency of operation is allowed in the fixed data rate mode.

Variable Data Rate Mode

Variable data rate timing is selected by connecting DCLKr to the bit clock for the receive PCM highway rather than to Vbb. It employs master clock CLK, bit clocks DCLKr and DCLKx, and frame synchronization clocks FSr and FSx.

Variable data rate timing allows for a flexible data frequency. It provides the ability to vary the frequency of the bit clocks, from 64 kHz to 2.048 MHz. The master clock is still restricted to 2.048 MHz.

In this mode, DCLKr and DCLKx become the data clocks for the receive and transmit PCM highways. While FSx is high, PCM data from Dx is transmitted onto the highway on the next eight consecutive positive transitions of DCLKx. Similarly, while FSr is high, each PCM bit from the highway is received by Dr on the next eight consecutive negative transitions of DCLKr.

TABLE 1 - Power-Down Methods

Device Status	Power-Down Method	Typical Power Consumption	Digital Output Status
Power Down Mode	$\overline{PDN}$ = TTL low	5 mW	$\overline{TS}$x and Dx are placed in a high impedance state within 10 us.
Standby Mode	FSx and FSr are are TTL low	12 mW	$\overline{TS}$x and Dx are placed in a high impedance state within 300 milliseconds.
Only transmit is on standby	FSx is TTL low	70 mW	$\overline{TS}$x and Dx are placed in a high impedance state within 300 milliseconds.
Only receive is on standby	FSr is TTL low	110 mW	

On the transmit side, the PCM word will be repeated in all remaining timeslots in the 125 us frame as long as DCLKx is pulsed and FSx is held high. This feature allows the PCM word to be transmitted to the PCM highway more than once per frame, if desired, and is only available in the variable data rate mode.

Precision Voltage Reference

No external components are required with the CODEC to provide the voltage reference function. Voltage references are generated on-chip and are calibrated during the manufacturing process. The technique uses a difference in sub-surface charge density between two suitably implanted MOS devices to derive a temperature and bias stable reference voltage. These references determine the gain and dynamic range characteristics of the device.

Separate references are supplied to the transmit and receive sections and each is trimmed independently during the manufacturing process. The reference value is then further trimmed in the gain setting op-amps to a final precision value.

TRANSMIT OPERATION

Transmit Filter

The input section provides gain adjustment in the passband by means of an on-chip operational amplifier. This operational amplifier has a common mode range of $\pm$2.17 volts, a maximum DC offset of 25 mV, a minimum open loop voltage gain of 5000, and a unity gain bandwidth of typically 1 MHz. Gain of up to 20 dB can be set without degrading the performance of the filter. The load impedance to ground (GRDA) at the amplifier output (GSx) must be greater than 10 kilohms in parallel with less than 50 pF. The input signal on lead VFxI- can be either AC or DC coupled.

A low pass anti-aliasing section is included on-chip. This section typically provides 35 dB attenuation at the sampling frequency. No external components are required to provide the necessary anti-aliasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation.

A high pass section configuration was chosen to reject low frequency noise from 50 and 60 Hz power lines, 17 Hz European electric railroads, ringing frequencies and their harmonics, and other low frequency noise. Even though there is high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

Encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor. The encoder then performs an analog to digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

An on-chip autozero circuit corrects for DC-offset on the input signal to the encoder. This autozero circuit uses the sign bit averaging technique; the sign bit from the encoder output is long term averaged and subtracted from the input to the encoder. In this way, all DC offset is removed from the encoder input waveform.

RECEIVE OPERATION

Decoding

The PCM word at the Dr lead is serially fetched on the first eight data clock bits of the frame. A D/A conversion is performed on the digital word and the corresponding analog sample is held on an internal sample and hold capacitor. This sample is then transferred to the receive filter.

Receive Filter

The receive filter provides passband flatness and stopband rejection.

Receive Output Power Amplifiers

A balanced output amplifier is provided in order to allow maximum flexibility in output configuration. Either of the two outputs can be used single ended (referenced to GRDA) to drive single ended loads. Alternatively, the differential output will drive a bridged load directly. The output state is capable of driving loads as low as 300 ohms single ended or 600 ohms differentially.

The receiver output (DISC OUT) and microphone output (MIC IN) are applied to A6-14 and A6-15. After processing, the DISC OUT and MIC IN signals are applied to the TRS board as RX AUDIO and TX AUDIO. DR and DX are the data receive and data transmit lines from the digital processor.

The CODEC also receives outputs from counter, A7. The inputs include the transmit synchronization clock (FSx) receiver synchronization clock (FSr), transmit and receive data clocks (DCLKx and DCLKr), and master clock (CLK).

COUNTER A7

Counter A7 is a 12-stage, binary counter that provides the time base for CODEC A6 and digital processor A5. The counter receives the master clock input from the microprocessor oscillator Y1.

In addition to the clock outputs to CODEC A6 and the digital processor, the counter also applies a 32 kHz output to timer A21 to provide the analog -5 volts (-5 AV) for the CODEC.

±5 VOLT (AV) REGULATOR

Two 5-volt regulators are used to supply power to CODEC A6. Switched A+ is applied directly to the +5 AV (analog voltage) regulator A17 which in turn supplies the CODEC. The negative 5 Volts is generated by a power supply consisting of timer A21, rectifier CR3, and -5 VDC regulator A18. A 32 kHz signal from high speed counter A7 is applied to rectifiers CR3. The rectified negative voltage is applied to -5 volt regulator A18 which then supplies a regulated -5 AV to CODEC A6. The ±5-volt supply is also applied to the tri-stage bilateral gate A19.

EEPROM "WRITE" CONTROL

The EEPROM "WRITE" (WR) control consists of Q10 and Q11. When address bit A10 from the microprocessor is high, Q10 turns on and Q11 turns off. This applies +5 volts to the WR input which disables the "WRITE" function. When address bit A10 goes low, Q10 turns off and Q11 turns on. This applies a low to the WR input, enabling the WRITE function (if CS is low) which allows data to be written to the EEPROM. To WRITE to the memory, the WRITE input must be low, and the OE input must be high. In the RD mode, write is high OE is low, and CS is low.

The WR function can also be enabled by a low from programmer TQ2310 via SP store.

AUDIO SWITCH A19

Transmit and receiver audio signals at J3 are routed to and from the CODEC through a three-stage bilateral switch (A19). The switch stages are controlled by the D-PTT of the microprocessor. In the transmit mode, the MIC IN is processed and applied to buffer A20. The buffer output is coupled through MODULATION ADJUST R52 and applied to the VCO mod input on the TRS board.

In the receive mode (D-PTT low), DISC OUT from the receiver is processed and applied directly to the receiver audio amplifier at RX AUDIO.

The switch is supplied by the ±5 AV regulators.

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WORLD HEADQUARTERS • LYNCHBURG, VIRGINIA 24502 U.S.A.

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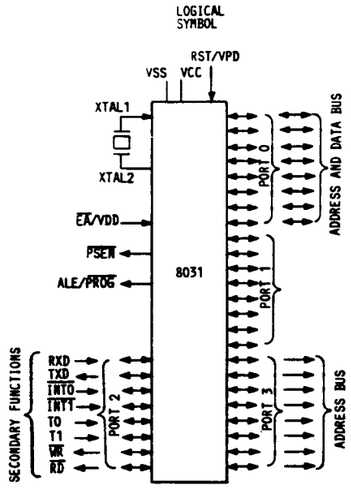
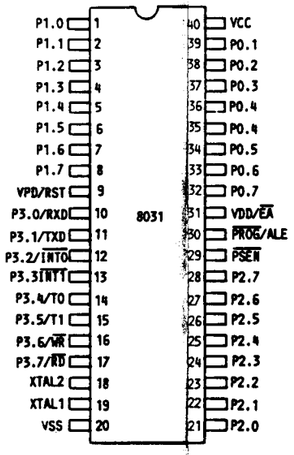
MICROPROCESSOR A1

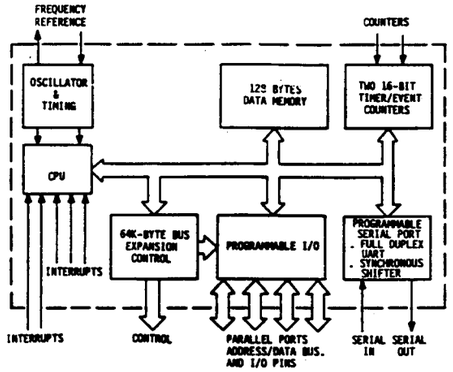
LOGICAL SYMBOL



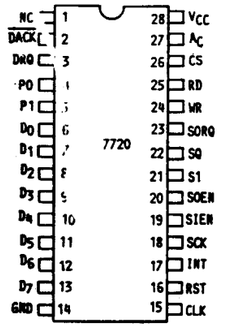
PIN CONFIGURATION



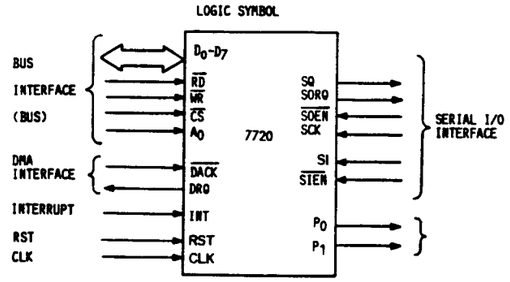
BLOCK DIAGRAM



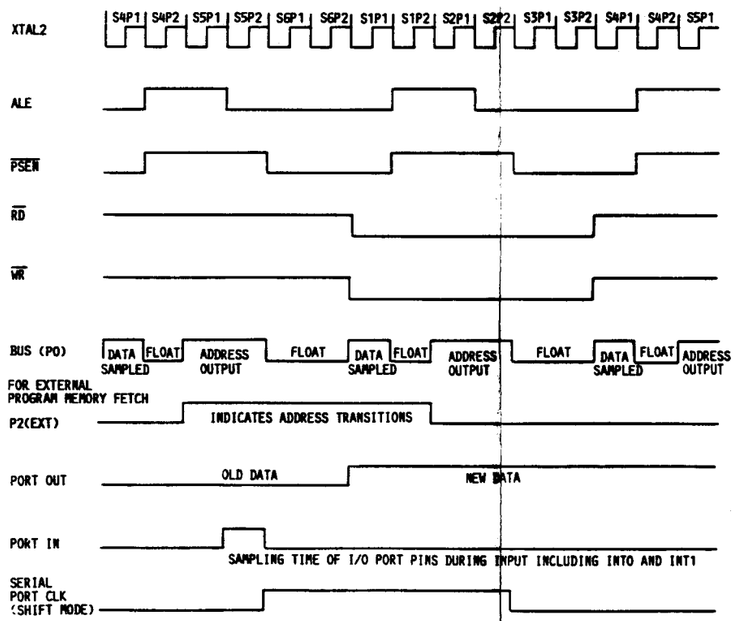
DIGITAL PROCESSOR A5



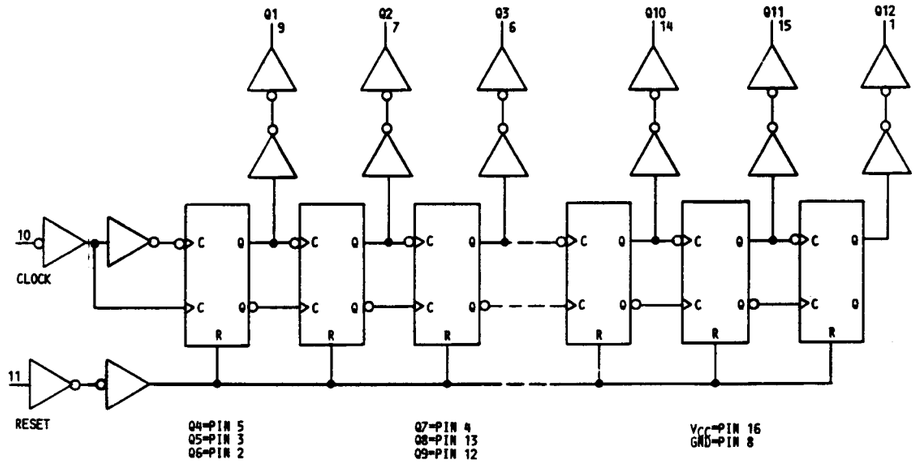
LOGIC SYMBOL



WAVEFORMS



COUNTER A7 (4040)



FUNCTION TABLE

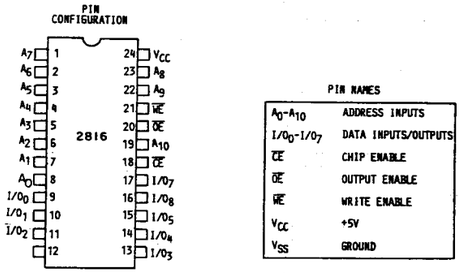
CLOCK	RESET	OUTPUT STATE
⌐	L	NO CHANGE
¬	L	ADVANCE TO NEXT STATE
X	H	ALL OUTPUTS ARE LOW

RC-5191

SERVICE SHEET

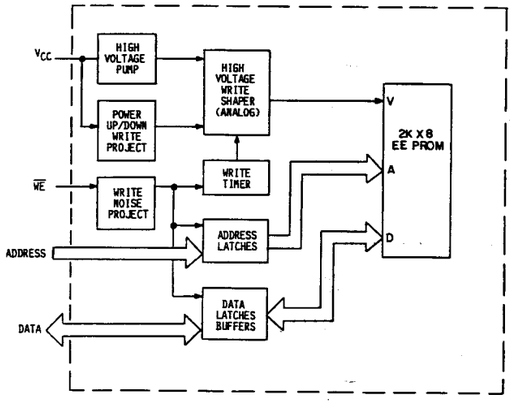
INTEGRATED CIRCUITS
(Sheet 1 of 2)

EE PROM A4

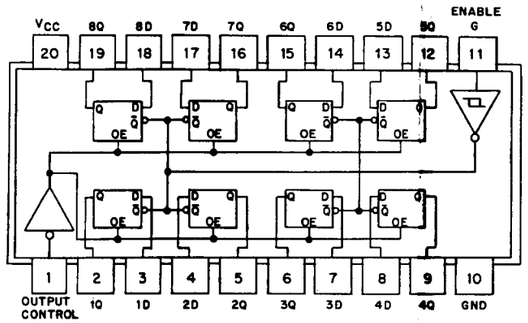


PIN NAMES	
A_0-A_{10}	ADDRESS INPUTS
I/O_0-I/O_7	DATA INPUTS/OUTPUTS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
V_{CC}	+5V
V_{SS}	GROUND

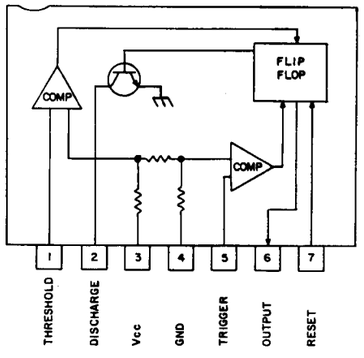
FUNCTIONAL DIAGRAM



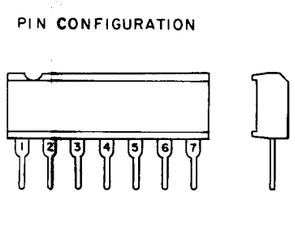
OCTAL LATCH A2, A11



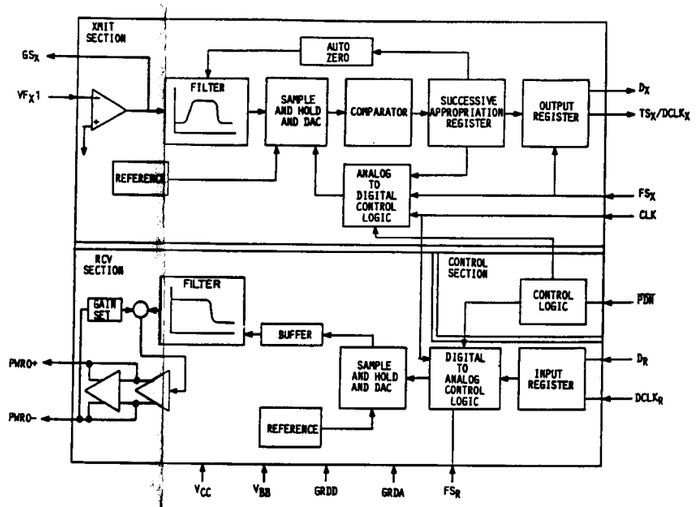
TIMER A21



PIN CONFIGURATION



CODEC A6



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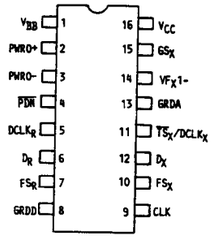


PIN NAMES	
V_{BB}	POWER (-5V)
PWRO+, PWRO-	POWER AMPLIFIER OUTPUTS
$\overline{PDN}$	POWER DOWN SELECT
$DCLK_R$	RECEIVE VARIABLE DATA CLOCK
D_R	RECEIVE PCM INPUT
FS_R	RECEIVE FRAME
	SYNCHRONIZATION CLOCK
GRDD	DIGITAL GROUND
V_{CC}	POWER (+5V)

PIN NAMES	
GS_X	TRANSMIT GAIN CONTROL
VF_X1-	ANALOG INPUT
GRDA	ANALOG GROUND
$\overline{TS_X}$	TIMESLOT STROBE/BUFFER ENABLE
$DCLK_X$	TRANSMIT VARIABLE DATA CLOCK
D_X	TRANSMIT PCM OUTPUT
FS_X	TRANSMIT FRAME
	SYNCHRONIZATION CLOCK
CLK	MASTER CLOCK

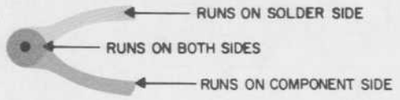
RC-5192A

SERVICE SHEET

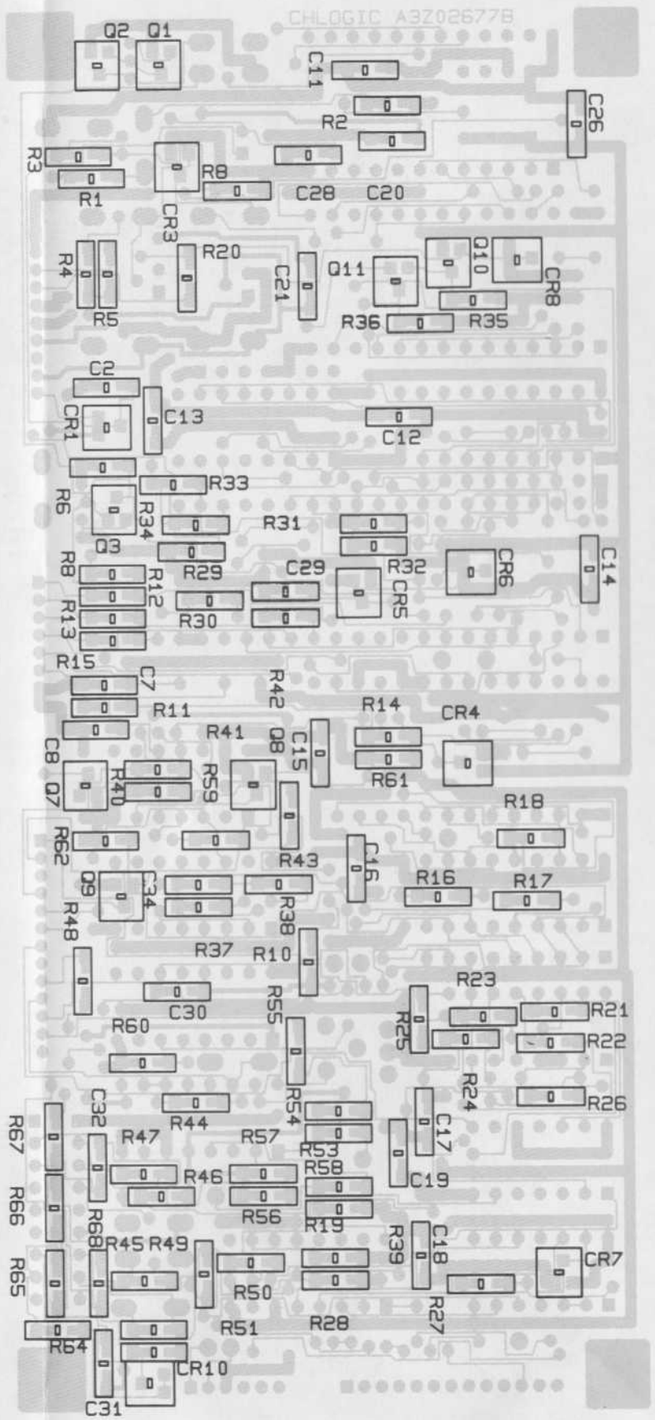
INTEGRATED CIRCUITS
(Sheet 2 of 2)

CAUTION

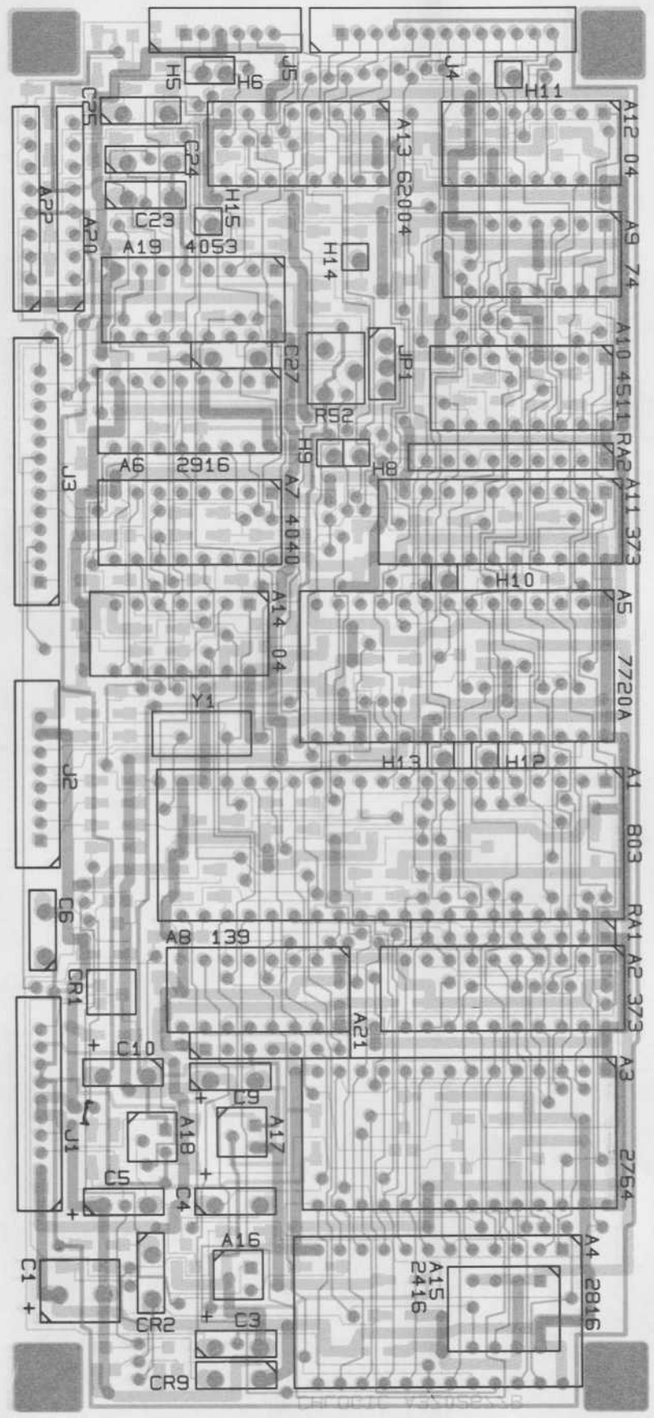
OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES



SOLDER SIDE

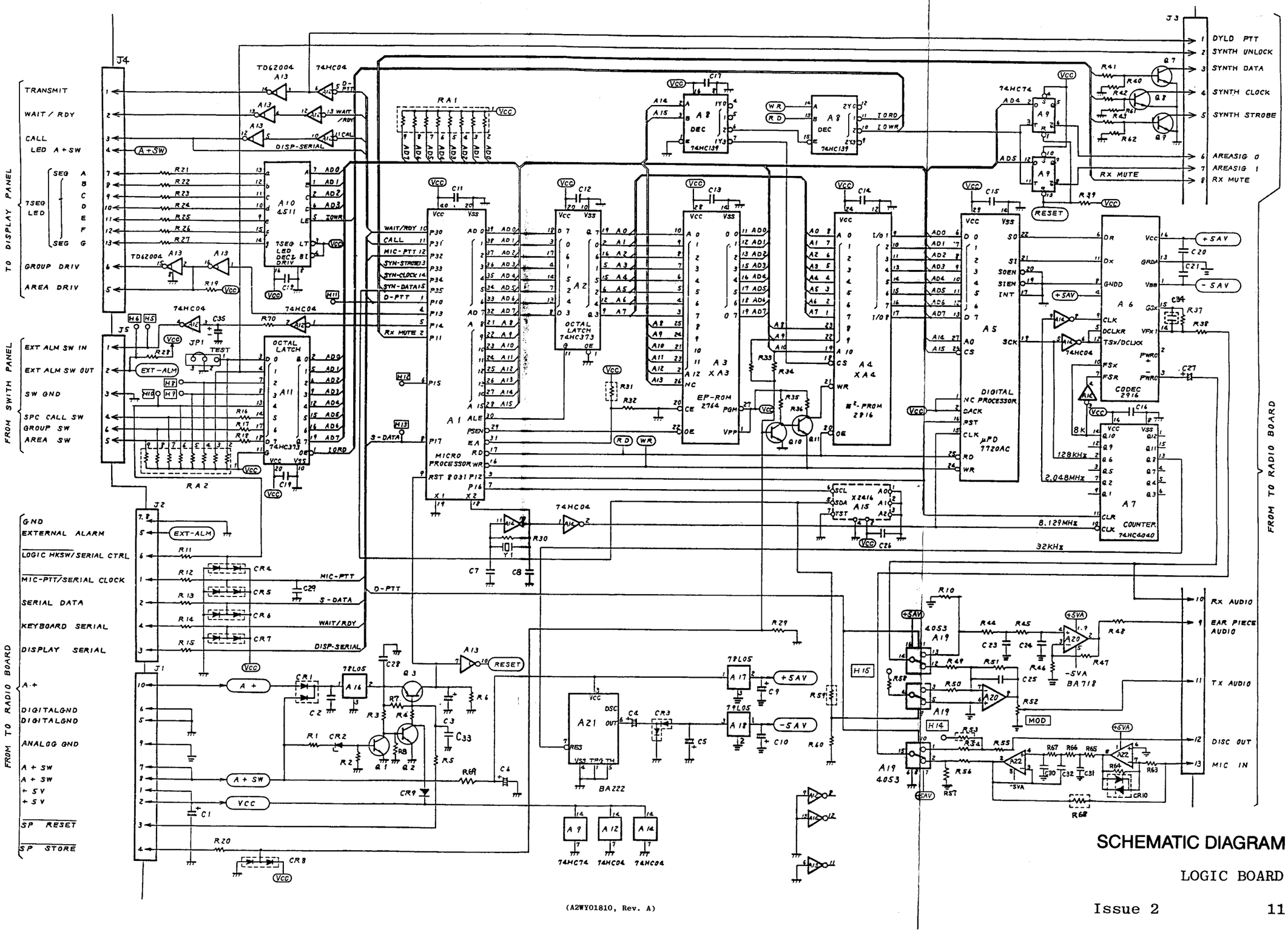


COMPONENT SIDE



OUTLINE DIAGRAM

LOGIC BOARD



(A2WY01810, Rev. A)

SCHEMATIC DIAGRAM

LOGIC BOARD

PARTS LIST

LOGIC BOARD
A4WE03583
ISSUE 2

SYMBOL	PART NO.	DESCRIPTION
		- - - - - - - - - INTEGRATED CIRCUITS - - - - - - - - -
A1	KEC/2ADA005179	Micro Processor P8031AH.
A2	KEC/2ABD018102	TC74HC373P
A3	KEC/2ACA033108	EP-ROM M5L2764K
A4	KEC/2ACA040087	EE PROM
A5		upD7720D-126
A6	KEC/2AAH019021	CODEC
A7	KEC/2ABD018512	TC74HC4040P
A8	KEC/2ABD018078	TC74HC139P
A9	KEC/2ABD018052	TC74HC74P
A10	KEC/2ABC057044	TC4511BP
A11	KEC/2ABD018102	TC74HC373P
A12	KEC/2ABD018169	TC74HC04P
A13	KEC/2AAG021014	TD62004P
A14	KEC/2ABD018169	TC74HC04P
A16 and A17	KEC/2AAE049161	VTG-REG AN78L05
A18	KEC/2AAE049179	VTG-REG AN79L05
A19	KEC/2ABC037012	TC4053BP
A20	KEC/2AAB020011	BA718
A21	KEC/2AAH039015	BA222
A22	KEC/2ABC037012	BA718
		- - - - - - - - - - CAPACITORS - - - - - - - - - -
C1	KEC/2CBJ001270	Fixed, elect Al KMA10VB100M.
C2	KEC/2CAK005391	Ceramic chip, 0.01 uF.
C3	KEC/2CCF001512	Fixed, tantalum 204M3502-105MB ±20%.
C4 thru C6	KEC/2CCD025012	Fixed, tantalum 204M3502-106M ±20%.
C7	KEC/2CAK005235	Ceramic chip RH 47P ±0.5 pF, 50V.
C8	KEC/2CAK005110	Ceramic chip CH 10P ±0.5 pF, 50V.
C9 and C10	KEC/2CCF001520	Fixed, tantalum 204M3502-106M ±20%.
C11 thru C22	KEC/2CAK005391	Ceramic chip, 0.01 uF 10%, 50V.
C23 and C24	KEC/2CDC001012	Fixed, film, ECQ-V1H104JZ9 0.1 uF ±5%, 50V.
C25	KEC/2CDC001087	Fixed, film, ECQ-B1H102JZ9 1000 pF ±5%, 50V.
C26	KEC/2CAK005391	Ceramic chip, 0.01 uF ±10%, 50V.
C27	KEC/2CCF003041	Fixed, tantalum 204M3502-106M ±20%.
C28	KEC/2CAK005391	Ceramic chip, 0.01 uF ±10%, 50V.
C29	KEC/2CAK005250	Ceramic chip, 100 pF RH ±5%, 50V.
C30	KEC/2CAK005151	Ceramic chip, 22 pF CH ±5%, 50V.
C31	KEC/2CAK005292	Ceramic chip, 470 pF RH ±5%, 50V.
C32	KEC/2CAK005529	Ceramic chip, 2200 pF ±10%, 50V.
C33	KEC/2CAK005230	Ceramic chip, 47 pF RH ±5%, 50V.
C35	KEC/CCF001470	Fixed, tantalum, 204M1602-475M.

SYMBOL	PART NO.	DESCRIPTION
		- - - - - - - - - - DIODES - - - - - - - - - -
CR1	KEC/2QBE005011	Silicon DAN202K.
CR2	KEC/2QBB001737	Zener HZ-7B1.
CR3 thru CR8	KEC/2QBE005037	Silicon DA204K.
CR9	KEC/2QBA006161	Silicon 1S2075K.
CR10	KEC/2QBE005037	Silicon DA204K.
		- - - - - - - - - - CONNECTOR - - - - - - - - - -
J1	KEC/2PDA012026	IL-S-10P-S2T2-EF
J2	KEC/2PDA012018	IL-S-8P-S2T2-EF
J3 and J4	KEC/2PDA012034	IL-S-13P-S2T2-EF
J5	KEC/2PDA012281	IL-S-6P-S2T2-EF
JP1	KEC/2PDD003774	PS-3PF-S4T1-KL1
P1	KEC/2PDE002056	PS-2SH4-1
		- - - - - - - - - - TRANSISTORS - - - - - - - - - -
Q1 and Q2	KEC/2QAD001039	Silicon 2SC2412LC.
Q3	KEC/2QAA011390	Silicon 2SA1201SC.
Q7 thru Q11	KEC/2QAD001039	Silicon 2SC2412LC.
		- - - - - - - - - - RESISTORS - - - - - - - - - -
R1 thru R5	KEC/2RGC001275	Square chip, 1/8W, 47K ohm ±5%.
R6	KEC/2RGC001242	Square chip, 1/8W, 22K ohm ±5%.
R7	KEC/2RGC001218	Square chip, 1/8W, 100K ohm ±5%.
R8	KEC/2RGC001275	Square chip, 1/8W, 47K ohm ±5%.
R10	KEC/2RGC001275	Square chip, 1/8W, 47K ohm ±5%.
R11 thru R15	KEC/2RGC001119	Square chip, 1/8W, 220 ohm ±5%.
R16 thru R19	KEC/2RGC001218	Square chip, 1/8W, 10K ohm ±5%.
R20	KEC/2RGC001119	Square chip, 1/8W, 220 ohm ±5%.
R21 thru R27	KEC/2RGC001093	Square chip, 1/8W, 100 ohm ±5%.
R28	KEC/2RGC001275	Square chip, 1/8W, 47K ohm ±5%.
R29	KEC/2RGC001176	Square chip, 1/8W, 2.2K ohm ±5%.
R30	KEC/2RGC001341	Square chip, 1/8W, 470K ohm ±5%.
R31	KEC/2RGC001218	Square chip, 1/8W, 10K ohm ±5%.
R32	KEC/2RGC001028	Square chip, 1/8W, 10 ohm ±5%.
R33 thru R36	KEC/2RGC001218	Square chip, 1/8W, 10K ohm ±5%.
R37	KEC/2RGC001275	Square chip, 1/8W, 47K ohm ±5%.
R38	KEC/2RGC001242	Square chip, 1/8W, 22K ohm ±5%.
R39	KEC/2RGC001275	Square chip, 1/8W, 47K ohm ±5%.
R40	KEC/2RGC001242	Square chip, 1/8W, 22K ohm ±5%.
R41 thru R43	KEC/2RGC001275	Square chip, 1/8W, 47K ohm ±5%.
R44	KEC/2RGC001176	Square chip, 1/8W, 2.2K ohm ±5%.
R45 and R46	KEC/2RGC001218	Square chip, 1/8W, 10K ohm ±5%.

SYMBOL	PART NO.	DESCRIPTION
R47	KEC/2RGC001309	Square chip, 1/8W, 100K ohm ±5%.
R48	KEC/2RGC001127	Square chip, 1/8W, 330 ohm ±5%.
R49 and R50	KEC/2RGC001218	Square chip, 1/8W, 10K ohm ±5%.
R51	KEC/2RGC001242	Square chip, 1/8W, 22K ohm ±5%.
R52	KEC/2RFB017068	Variable, 10K ohm ±30%, Mod Adjust.
R53	KEC/2RGC001010	Square chip, 1/8W, 0 ohm ±5%.
R54	KEC/2RGC001275	Square chip, 1/8W, 47K ohm ±5%.
R55	KEC/2RGC001010	Square chip, 1/8W, 0 ohm ±5%.
R56 and R57	KEC/2RGC001189	Square chip, 1/8W, 3.3K ohm ±5%.
R58	KEC/2RGC001010	Square chip, 1/8W, 0 ohm ±5%.
R59	KEC/2RGC001275	Square chip, 1/8W, 47K ohm ±5%.
R60	KEC/2RGC001036	Square chip, 1/8W, 10 ohm ±5%.
R61 and R62	KEC/2RGC001242	Square chip, 1/8W, 22K ohm ±5%.
R63	KEC/2RGC001275	Square chip, 1/8W, 47K ohm ±5%.
R64	KEC/2RGC001218	Square chip, 1/8W, 100K ohm ±5%.
R65 thru R67	KEC/2RGC001317	Square chip, 1/8W, 150K ohm ±5%.
R68	KEC/2RGC001010	Square chip, 0 ohm.
R69	KEC/2RGC001036	Square chip, 1/8W, 10 ohm ±5%.
R70	KEC/2RGC001309	Square chip, 1/8W, 100K ohm ±5%.
RA1 and RA2	KEC/2REA020116	EXB-P88-473K
		- - - - - - - - - - IC SOCKET - - - - - - - - - -
XA3	KEC/2PDH001241	IC03T-280684
XA4	KEC/2PDH001282	IC03T-240684
		- - - - - - - - - QUARTZ CRYSTAL - - - - - - - - -
Y1	KEC/2YAA181632	HC-43/U-4, 8.192 MHz.

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES.